

IN THE CLAIMS:

1. (Currently Amended) A method of forming at least one field effect transistor on a substrate, the method comprising:

forming a gate insulation layer for said at least one field effect transistor on a surface of said substrate;

after forming said gate insulation layer, forming a strained surface layer on a surface of said substrate by implanting ions of at least one heavy inert material through said gate insulation layer and said surface of said substrate;

forming at least one gate structure above said strained surface layer; and

performing additional process steps to manufacture said at least one field effect transistor, wherein a thermal budget in manufacturing the at least one field effect transistor is adjusted to substantially avoid silicon grid restoration in the strained surface layer.

2. (Original) The method of claim 1, wherein ions of at least one of xenon, argon, germanium, silicon, or a combination thereof, are implanted.

3. (Original) The method of claim 1, wherein the implanting energy is selected in the range of approximately 10-100 keV.

4. (Original) The method of claim 1, wherein the implanting dose is selected in the range of approximately $10^{13}/\text{cm}^2 - 10^{16}/\text{cm}^2$.

5. (Canceled)

6. (Original) The method of claim 1, wherein said substrate comprises one of silicon and germanium or a combination thereof.

7. (Original) The method of claim 1, wherein said field effect transistor is one of an NMOS, a PMOS and a CMOS transistor.

8.-17. (Canceled)

18. (Previously Presented) A method of forming at least one field effect transistor on a substrate, the method comprising:

forming a gate insulation layer for said at least one field effect transistor on a surface of said substrate;

forming a strained surface layer on a surface of said substrate by implanting ions of at least one heavy inert material through said gate insulation layer and into said substrate; and

forming at least one gate electrode structure above said gate insulation layer after forming said strained surface layer.

19. (Previously Presented) The method of claim 18, wherein ions of at least one of xenon, argon, germanium, silicon, or a combination thereof, are implanted.

20. (Previously Presented) The method of claim 19, further comprising performing additional process steps to manufacture said at least one field effect transistor, wherein a thermal budget in manufacturing the field effect transistor is adjusted to substantially avoid silicon grid restoration in the strained surface layer.

21. (Previously Presented) The method of claim 19, wherein said strained surface layer has a thickness less than 20 nm.